1. (Amended) An interrupt mask disable circuit comprising: [apparatus for disabling a masked interrupt wherein an interrupt is being requested by an assertion of an interrupt request signal, said apparatus comprising:]

first logic circuitry operably coupled to receive an interrupt request and a mask signal and to provide an interrupt signal when the interrupt request is active and the mask signal is disabled, and to provide a non-interrupt signal when the mask signal is enabled regardless of whether the interrupt request is active or inactive; and

second logic circuitry operably coupled to receive a mask activation signal and a mask override signal and to produce the mask signal, wherein the mask signal is enabled when the mask activation signal is active and the mask override signal is not enabled and wherein the mask signal is disabled when the mask override signal is active regardless of whether the mask activation signal is enabled or disabled.

[means for indicating a software condition;

means for indication a hardware condition; and

means for unmasking said masked interrupt in response to the assertion of said interrupt request signal and at least one of said indicated software condition and said indicted hardware condition.]

2. (amended) The interrupt mask disable circuit of claim 1, wherein the mask activation signal is enabled based on a software condition.

[An apparatus as recited in claim 1 wherein said means for unmasking comprises:

means for enabling an unmasking circuit in response to at least one of said indicated software condition and said indicated hardware condition; and

means for asserting said interrupt when said interrupt request signal is asserted and said unmasking circuit is enabled and for not asserting said interrupt when said interrupt request signal is asserted and said masking circuit is not enabled.]

3/4. The interrupt mask disable circuit of claim 1 further [An apparatus as recited in claim 1 wherein said means for indicating said software condition] comprises a programmable register that outputs the mask activation [a software enable] signal.

4/8. The interrupt mask disable circuit of claim 1, wherein the mask override signal is enabled based on a hardware condition.

[An apparatus as recited in claim 1 wherein said means for indicating said hardware condition comprises at least one hardware circuit, and wherein each of said at least one hardware circuit outputs a hardware enable signal.]

8/6. The interrupt mask disable circuit of claim 1, wherein the ~~first~~ second logic circuitry comprises [An apparatus as recited in claim 3 wherein said means for enabling said unmasking circuit comprises] an OR gate [that receives at least one of an indicated software condition enable signal and an indicated hardware condition enable signal and that outputs a combined enable signal].

9/7. The interrupt mask disable circuit of claim 1, wherein the ~~second~~ first logic circuitry comprises [An apparatus as recited in claim 26 wherein said means for asserting comprises] an AND gate [that receives said combined enable signal and said interrupt request signal and that outputs said interrupt].

8. The interrupt mask disable circuit of claim 5 further comprises being incorporated within a [An apparatus as recited in claim 7 wherein said apparatus is included in a] processor, and wherein the hardware condition occurs when [said at least one hardware circuit asserts said hardware enable signal when] said processor is in a particular state.

10. The interrupt mask disable circuit of claim 8, wherein the hardware condition occurs [An apparatus as recited in claim 7 wherein said apparatus is included in a processor, and wherein said at least one hardware circuit asserts said hardware enable signal] in response to an external enable signal generated external to said processor.

23. A processor comprising:

a microcontroller;

memory operably coupled to the microcontroller; and

interrupt control circuit that includes:

first logic circuitry operably coupled to receive an interrupt request and a mask signal and to provide an interrupt signal to the microcontroller when the interrupt request is active and the mask signal is disabled, and to provide a non-interrupt signal when the mask signal is enabled regardless of whether the interrupt request is active or inactive; and

second logic circuitry operably coupled to receive a mask activation signal and a mask override signal and to produce the mask signal, wherein the mask signal is enabled when the mask activation signal is active and the mask override signal is not enabled and

wherein the mask signal is disabled when the mask override signal is active regardless of whether the mask activation signal is enabled or disabled.

[In a processor that may enter a predetermined state from which it may only escape via an interrupt, and wherein while said processor is in said predetermined state all interrupts are masked, a circuit for unmasking a masked interrupt, said circuit comprising:

a first subcircuit that receives a first signal which indicates whether said processor is in said predetermined state and at least one of an external signal and a software enable signal, said first subcircuit produces an unmasking signal based on whether said first signal indicates said processor is in said predetermined state and whether at least one of said software enable signal and said external signal request an interrupt to be masked;

a second subcircuit that receives said unmasking signal and a first interrupt request signal, said second subcircuit produces a second interrupt request signal based on said unmasking signal and said first interrupt signal; and

a third subcircuit responsive to said interrupt signal for interrupting said processor.]

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27. A method for masking an interrupt, the method comprising the steps of:

a) receiving an interrupt signal;

b) determining whether a mask signal is enabled;

c) when the mask signal is enabled, determining whether a mask override signal is enabled; and

d) when the mask override signal is enabled, providing the interrupt signal to a processor regardless of whether the mask signal is enabled or disabled.

[An apparatus for generating an interrupt, said interrupt being requested by an assertion of an interrupt request signal, said apparatus comprising:

means for indicating a software condition comprising a programmable register that outputs a software enable signal;

means for indicating a hardware condition, said means for indicating said hardware condition comprises at least one hardware circuit, and wherein each of said at least one hardware circuit outputs a hardware enable signal; and

means for generating said interrupt in response to the assertion of said interrupt request signal and at least one of said indicated software condition and said indicated hardware condition, said means for generating comprising:

means for enabling said interrupt in response to said software condition and said hardware condition, said means for enabling said interrupt comprises an OR gate that receives said software enable signal and said hardware enable signal and that outputs a combined enable signal; and

means for asserting said interrupt when said interrupt request is asserted and said interrupt is enabled and for not asserting said interrupt when said interrupt request is asserted and said interrupt is not enabled.]